In the Claims:

1. (Currently Amended) A semiconductor memory device, comprising:

a plurality of unit memory cells, wherein a unit memory cell comprises:

a first planar transistor in a semiconductor substrate; ~~and~~

a vertical transistor disposed on the first planar transistor; and

a second planar transistor in the semiconductor substrate, wherein the second planar transistor is electrically connected in series with the first planar transistor.

2. (Currently Amended) The semiconductor memory device of Claim 1, wherein ~~the~~ each unit memory cell further comprises:

first and second conductive regions formed in the semiconductor substrate to define a channel region;

a storage node, a multi-junction storage pattern and a data line, which are sequentially stacked on the semiconductor substrate; and

a word line crossing over the data line and covering both sidewalls of the multi-junction storage pattern. ~~semiconductor memory device further comprises a plurality of word lines.~~

3. (Currently Amended) The semiconductor memory device of Claim 2, wherein the first planar transistor comprises the storage node, the first and second conductive regions and the channel region,

the vertical transistor comprises the word line, the storage node, the data line and the multi-junction storage pattern, and

the second planar transistor comprises the word line, the first and second conductive regions and the channel region. ~~one of the word lines comprises a gate of the second planar transistor~~.

4. (Currently Amended) The semiconductor memory device of Claim ~~1,~~ 3, wherein the word line is used as both a gate of the second planar transistor and a gate of the vertical

transistor. ~~first planar transistor includes a storage node, and wherein the storage node comprises the gate of the first planar transistor.~~

5. (Currently Amended) The semiconductor memory device of Claim ~~4,~~ 3, wherein the word line is configured to connect the second planar transistors and vertical transistors of the unit memory cells along a direction perpendicular to the data line. ~~storage node further comprises the source of the vertical transistor.~~

6. (Currently Amended) The semiconductor memory device of Claim ~~4,~~ 3, wherein the data line is an electrode of the vertical transistor, which is used to supply the storage node with electric charges or to drain electric charge from the storage node. ~~first planar transistor further comprises a first conductive region and a second conductive region~~.

7. (Currently Amended) The semiconductor memory device of Claim ~~6,~~ 3, wherein the data line is configured to connect the vertical transistors of the unit memory cells along a direction perpendicular to the word line. ~~first planar transistor further comprises a channel region disposed between the first conductive region and the second conductive region, and wherein the storage node is disposed only on a first portion of the channel region.~~

8. (Currently Amended) The semiconductor memory device of Claim ~~7,~~ 2, a portion of the first conductive region adjacent the channel is lightly doped as compared to a portion of the second conductive region adjacent the channel.

9. (Currently Amended) The semiconductor memory device of Claim ~~8,~~ 3, wherein the first and second planar transistors are connected in series with the first and second conductive regions. ~~the vertical transistor further comprises a multi-junction storage pattern on the storage node, a data line on the multi-junction storage pattern, and a word line that is on the data line.~~

10. (Currently Amended) The semiconductor memory device of Claim ~~9,~~ 3, wherein the channel region comprises a first channel region and a second channel region, and wherein

the first planar transistor is disposed on the first channel region and the second planar transistor is disposed on the second channel region. ~~word line is also on the second channel region.~~

11. (Currently Amended) The semiconductor memory device of Claim ~~9,~~ 2, further comprising a capping insulation pattern disposed on ~~between~~ the data line, the capping insulation pattern separating the data line from ~~and~~ the word line.

12. (Original) The semiconductor memory device of Claim 1, wherein the first planar transistor and the second planar transistor have different threshold voltages.

13-37. (Cancelled)

38. (Original) A semiconductor memory device, comprising:

a source region and a drain region in a semiconductor substrate;

a gate that is laterally offset from at least one of the source region and the drain region and provided on the substrate between the source region and the drain region;

a vertical transistor on the gate.

39. (Original) The semiconductor memory device of Claim 38, wherein the gate comprises a storage node.

40. (Original) The semiconductor memory device of Claim 39, wherein the storage node comprises a source/drain region of the vertical transistor.

41-44. (Canceled)

45. (Previously Presented) The semiconductor memory device of Claim 1, wherein a channel region of the second planar transistor comprises a portion of a channel region of the first planar transistor.

46. (Previously Presented) The semiconductor memory device of Claim 1, wherein

the first planar transistor and the second planar transistor share a common source/drain region.

47. (New) The semiconductor memory device of Claim 38, wherein the gate comprises the gate of a first planar transistor in the semiconductor substrate, and wherein the semiconductor memory device further comprises a second planar transistor in the semiconductor substrate that is electrically connected in series with the first planar transistor.

48. (New) The semiconductor memory device of Claim 47, further comprising a word line crossing over the data line and covering both sidewalls of the multi-junction storage pattern and, wherein the vertical transistor comprises the gate which acts as a storage node, a multi-junction storage pattern, a data line and the word line, which are sequentially stacked on the semiconductor substrate, and wherein.

49. (New) The semiconductor memory device of Claim 48, wherein the word line is used as both a gate of the second planar transistor and a gate of the vertical transistor.

50. (New) The semiconductor memory device of Claim 49, wherein the data line is an electrode of the vertical transistor, which is used to supply the storage node with electric charges or to drain electric charge from the storage node.

51. (New) The semiconductor memory device of Claim 49, wherein the data line is configured to connect the vertical transistors of the unit memory cells along a direction perpendicular to the word line.

52. (New) The semiconductor memory device of Claim 49, wherein the source region and the drain region define a channel region that comprises a first channel region and a second channel region,

wherein the first planar transistor is disposed on the first channel region and the second planar transistor is disposed on the second channel region.

53. (New) The semiconductor memory device of Claim 48, further comprising a capping insulation pattern disposed on the data line, the capping insulation pattern separating the data line from the word line.

54. (New) The semiconductor memory device of Claim 47, wherein the first planar transistor and the second planar transistor have different threshold voltages.